PATENT
Attorney Docket No.: SAM-0210

In the claims:

Please amend claim 1 as follows:

1. (Twice Amended) A fuse circuit for a semiconductor integrated circuit, comprising:

a plurality of fuses; and

a plurality of transmission circuits, each transmission circuit being coupled to a corresponding fuse of the plurality of fuses; each transmission circuit for transferring signals from an input node to an output node in response to a status of the corresponding fuse, the input and output nodes of respective transmission circuits being coupled such that the transmission circuits are arranged in series.

REMARKS

Claims 1-12 are pending in the present application. Claim 1 is amended above. no new matter is added. Entry is respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification by the current Amendment. The attached page is captioned **"Version with Markings to Show Changes Made"**.

The abstract of the disclosure section of the specification stands objected to for reasons stated in the Office Action. The abstract is amended above in a manner that is consistent with suggestions made in the Office Action. Entry of the amendment and removal of the objection are respectfully requested.

Claims 1-12 stand rejected under 35 U.S.C. 102(b) as being anticipated by Kubota. Reconsideration of this rejection and allowance of the claims are respectfully requested in view of the foregoing amendments and the following remarks.

The present invention of amended claim 1 is directed to a fuse circuit for a semiconductor integrated circuit. The fuse circuit includes a plurality of fuses; and a plurality of transmission circuits. Each transmission circuit is coupled to a corresponding fuse of the plurality of fuses. Each transmission circuit transfers signals from an input node to an output node in response to a status of the corresponding fuse, the input and output nodes of respective transmission circuits being coupled such that the transmission circuits are arranged in series.

The present invention of claim 8 is directed to a fuse circuit storing information related to a semiconductor integrated circuit. The fuse circuit includes a plurality of fuses each of which has first and second terminals. The first terminal of each is connected to a power supply voltage. Each fuse stores predetermined information relevant to the semiconductor integrated circuit. The fuse circuit further includes a plurality of transmission circuits. Each transmission circuit is connected to a second terminal of a corresponding fuse of the plurality of fuses. Each transmission circuit transfers an input signal received at an input terminal to an output terminal in response to the predetermined information established by a status of the corresponding fuse. The transmission circuits are connected in series.

Thus, in the inventions as defined by claim 1 and 8, the input nodes and output nodes of respective transmission circuits are connected in series. In this manner, each transmission circuit transfers signals "from an input node to an output node in response to a status of the corresponding fuse" (claim 1), or each transmission circuit transfers "an input signal received at an input terminal to an output terminal in response to the predetermined information established by a status of the corresponding fuse" (claim 8).

The Office Action states, at section 5, paragraph 4 that "each of the transmission circuits" of Kubota "should be interpreted as the entire circuit block 21 less the fuse in that circuit block, i.e. the transmission gate is only one element in the transmission circuit". It is further stated that "based on this interpretation, it is clear that each transmission circuit has an input node (left) and an output node (right), and the configuration clearly shows a series arrangement".

In response to this assertion, the applicant respectfully submits that assuming each circuit block 21 of FIG. 6 of Kubota to be interpreted as a "transmission circuit" having an "input node" at the left side of each dashed-line box 21, and an "output node" at the right side of each dashed-line box 21, and therefore the "transmission circuits" of Kubota are connected in series, as indicated by the Office Action, then it follows that any signal that is presented to the "input node" of each Kubota "transmission circuit" 21 will be the same exact signal at the "output node" of that same Kubota "transmission circuit" 21, since, under this interpretation, the "input node" and "output node" of each individual Kubota "transmission circuit" are directly tied together on line V_G.

Following this line of reasoning, this interpretation of Kubota fails to teach or suggest each transmission circuit transferring signals "from an input node to an output node in response to a status of the corresponding fuse", as claimed in claim 1 of the present invention, and fails to teach or suggest each transmission circuit transferring "an input signal received at an input terminal to an output terminal in response to the predetermined information established by a status of the corresponding fuse", as claimed in claim 8, since the Kubota embodiment transfers whatever signal is present at the "input node" (left side of box 21) directly to the "output node" (right side of box 21), irrespective of the status of any fuse, since the "input node" and "output node" are directly coupled together in the Kubota embodiments.

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In view of the above, it is submitted that Kubota fails to anticipate the present invention as claimed in claims 1 and 8. Reconsideration of the rejection and allowance of claims 1 and 8 are therefore respectfully requested. With regard to the various dependent claims 2-7 and 9-12, it follows that these claims should inherit the allowability of the independent claims from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900, Ext. 4902
Facsimile: (617) 742-7774
J:\SAM\0210\210amendmentb.wpd

Anthony P. Onello, Jr.
Registration Number 38,572
Attorney for Applicant

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Version with Markings to Show Changes Made

In the specification:

The abstract of the invention section of the specification is amended above as follows:

(Twice Amended) In a fuse circuit including programmable fuses in a semiconductor integrated circuit, the fuses store specific information related to the semiconductor integrated circuit, such as redundancy information, wafer lot number, die lot number, and die position on the wafer, etc. The fuse circuit utilizes a plurality of fuses for storing identical bit information. Consequently, in the case where a fuse has not been cut out correctly, the fuse circuit [of the present invention] can reduce programming defects, whereby defect generation rates are remarkably decreased.

In the Claims:

Claim 1 is amended above as follows:

1. (Twice Amended) A fuse circuit for a semiconductor integrated circuit, comprising:

a plurality of fuses; and

a plurality of transmission circuits, each transmission circuit being coupled to a corresponding fuse of the plurality of fuses; each transmission circuit for transferring signals from an input node to an output node in response to a status of the corresponding fuse, the input and output nodes of respective [adjacent] transmission circuits being coupled such that the transmission circuits are arranged in series.